LISTING OF THE CLAIMS

1-87. (Canceled)

88. (Previously Presented) A process for forming an interposer element for use as a chip carrier comprising the steps of:

providing an insulating layer on at least one surface of a silicon substrate; and

processing said insulating layer to produce at least one passive circuit element on or within said insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of said insulating layer having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate,

solder bonding at least one integrated circuit chip to said interposer element, by forming a plurality of individual solder ball leads, wherein two or more of said individual solder ball leads use differing types of solder having differing melting points, such that said at least one integrated circuit chip is electrically connection to said at least one passive circuit element; and

forming a metallization pattern on or within said insulating layer, said metallization pattern being connected with said at least one passive circuit element.

89-91. (Canceled)

92. (Original) The process according to claim 89, wherein said insulating layer is formed of an oxide.

93. (Original) The process according to claim 92, wherein said oxide is silicon dioxide (SiO2).

94. (Original) The process according to claim 93, wherein said insulating layer has a thickness within a range of three to five microns.

95. (Original) The process according to claim 89, wherein said insulating layer is formed of polyamide.

96. (Canceled)

97. (Original) The process according to claim 96, wherein said step of processing said insulating layer further comprises the step of producing a plurality of passive circuit elements on or within said insulating layer.

98. (Original) The process according to claim 97, wherein said plurality of passive circuit elements includes a resistor element.

99. (Original) The process according to claim 98, wherein said resistor element is a thin film metal resistor.

100. (Original) The process according to claim 97, wherein said plurality of passive circuit elements includes a capacitor element.

101. (Original) The process according to claim 100, wherein said capacitor element is a thin film capacitor.

102. (Original) The process according to claim 101, wherein said thin film capacitor includes a dielectric layer.

103. (Original) The process according to claim 102, wherein said dielectric layer is an oxide composition.

104. (Original) The process according to claim 102, wherein said dielectric layer is an oxide-nitride-oxide composition.

105. (Original) The process according to claim 97, wherein said plurality of passive circuit elements includes an inductor element.

106. (Original) The process according to claim 105, wherein said inductor element is a spiral inductor.

107. (Original) The process according to claim 97, further comprising the step of forming at least one passive circuit device for use in radio frequency (RF) communications systems, said passive circuit device having at least one of said plurality of passive circuit elements and electrically connected to said at least one integrated circuit chip.

108. (Original) The process according to claim 107, further comprising the step of arranging the interposer element and said at least one integrated circuit to form circuitry for use in RF communications systems.

109. (Original) The process according to claim 108, wherein said at least one passive circuit device is for use in a load amplifier.

110. (Original) The process according to claim 108, wherein said at least one passive circuit device is for use in a broad band amplifier.

111. (Original) The process according to claim 108, wherein said at least one passive circuit device is for use in an oscillator.

112. (Original) The process according to claim 111, wherein said oscillator is a voltage controlled oscillator.

113. (Original) The process according to claim 108, wherein said at least one integrated circuit chip contains analog circuitry.

114. (Original) The process according to claim 108, wherein said at least one integrated circuit chip contains digital circuitry.

115. (Original) The process according to claim 114, wherein said integrated circuit chip is a microprocessor.

116. (Original) The process according to claim 114, wherein said integrated circuit chip is a memory chip.

117. (Original) The process according to claim 108, further comprising the step of forming a bonding layer, said bonding layer located in the area between said at least one integrated circuit chip and said insulating layer.

118. (Original) The process according to claim 117, wherein said bonding agent is epoxy.

119. (Original) The process according to claim 118, further comprising the step of encapsulating the interposer element and said at least one integrated circuit to form a circuit package, said circuit package having conducting leads on an outer side of said package.

120. (Original) The process according to claim 119, further comprising the step of providing conductive leads connecting the interposer element and said at least one integrated circuit to said conductive package leads of said circuit package.

121. (Original) The process according to claim 120, further comprising the step of providing an insulating layer to both surfaces of said silicon substrate.

122. (Canceled)

123. (Original) The process according to claim 88, said step of processing said insulating layer further comprising the step of providing at least one passive circuit element in each of a plurality of areas of said insulating layer, dividing said silicon substrate into said areas, and bonding at least one integrated circuit chip to each of said areas of said insulating layer to form respective chip carriers.

124. (Canceled)